



atta fin-1 (NE)

Docket No. 50265-0018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

David C. CHAPMAN

Examiner: A. Thompson

Serial No. 09/421,437

Filed: October 19, 1999

Croup Art Unit: 2825

Examiner: A. Thompson

For: APPROACH FOR ROUTING AN INTEGRATED CIRCUIT

Box AF Commissioner for Patents Washington, D.C. 20231 FAX COPY RECEIVED

MAY 2 2 2002

AMENDMENT AFTER FINAL REJECTION

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In response to the Final Office Action mailed July 11, 2001, please amend the application referenced above as indicated hereinafter. Pursuant to updated rule 37 C.F.R. § 1.121, the amended claim is provided in "clean form" below and a complete set of marked up claims showing the deletions and additions in the amended claim is provided on separate pages after this amendment.

- 1 21. (ONCE AMENDED) A method for automatically verifying an integrated circuit
- 2 layout, the method comprising the computer-implemented steps of:
- 3 receiving integrated circuit layout data that defines a set of two or more layout
- 4 objects contained in the integrated circuit layout;



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TO: Examiner Thompson	FROM: Edward A. Becker
COMPANY: USPTO Group Art Unit 2825	MAY 21, 2002
FAX NUMBER: 703-746-4112	TOTAL NO. OF PAGES INCLUDING COVER.
PHONE NUMBER: 703-305-7441	sender's reference number: 50265-0018
Amendment After Final	your reference number: 09/421,437

NOTES/COMMENTS:

Per your request and telephone message to Edward A. Becker, attached is the Amendment After Final Rejection that was faxed on September 10, 2001 (see attached Transmission Verification Report).

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PLEASE DELIVER IMMEDIATELY TO EXAMINER <u>A.M. THOMPSON</u>.

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